REMARKS

In response to the explanation given on pages 3-5 of the Final Office Action, Applicants amend claim 1 to overcome the anticipation rejection in view of U.S. Patent No. 6,370,661 issued to Miner ("Miner"). The amended material is from claim 8 which has been canceled. Although the Final Office Action provides a relatively careful analysis of the independent claims in comparing them to Miner, it fails to address the limitations of dependent claim 8 (now canceled) wherein *the first memory testing engine uses data, address, and control pathways used by the first bus controller so that if data traffic is being passed to a memory module by the first bus controller, the memory testing engine cannot run a test function*. This feature is not taught or suggested by Miner.

When interpreting Miner according to the Final Office Action, the Applicants claimed first memory testing engine is analogized to test execution logic 560, the first bus controller is allegedly present or is analogized to the test management logic 570, and the processor is analogized to the test controller 580. However, the Final Office Action has not identified which are the data, address, and control pathways that are used by the claimed first bus controller, as well as by the first memory testing engine, such that if data traffic is being passed to a memory module by the first controller, the memory testing engine cannot run a test function.

In Miner, there is an address/data bus 532 and a memory control bus 564 which is used to connect the logic 560 to the memory 510, as well as connect the logic 560 to a bus unit 530. Miner also states that the bus unit 530, which is the normal system interface, is disabled during test. However the Final Office Action has not used the bus unit 530 in the rejection, and instead has elected to interpret Applicants' claimed bus controller as reading on a portion of the test execution logic 570. Even assuming for the sake of argument that there could be a bus controller in the logic 570 (that is coupled to the bus 575), there is no teaching or suggestion that such a bus controller would use the data, address, and control pathways (address/data bus 532 and memory control 564), so that if data traffic is being passed to a memory 510 by the bus controller, the test executing logic 560 cannot run a test function. Even if there was such a bus controller within the test management logic 570, Miner does not suggest that such logic would

have the ability to pass data traffic to a memory module 510 without the execution logic 560 being involved. Accordingly, the mapping of Applicants' claim 1 with respect to Miner as indicated in the Final Office Action is flawed, as can be seen when considering the limitations of claim 8 which has now been incorporated into claim 1. Reconsideration and withdrawal of the rejection of claim 1 is therefore respectfully requested.

Turning now to claim 16, this claim has been amended with material from dependent claim 22 now canceled, reflecting the ability of passing control of data, address, and control pathways between a memory test engine and one of the bus controllers, so that only one of the two has control at one time. In Miner, however, there is no indication that control of the address/data bus 532 and memory control 564 is passed between the test execution logic 560 and a bus controller within the test management logic 570, so that only one of the two has control at one time. In fact, it is more likely that in Miner, control of the memory bus 532, 564 can only be initiated by using the test execution logic 560. In other words, the test execution logic 560 has control of the memory bus at all times where data traffic is being passed to memory. Accordingly, claim 16 as amended here is not anticipated or obvious in view of Miner.

Turning now to claim 30, this claim recites a sequence of instructions that are capable of performing a method in which a memory associated with an ASIC is accessed via a utility bus slave (UBS) controller over a bus. A memory test engine is configured by writing to the UBS controller over that bus. Miner, however, does not teach or suggest accessing such a memory. In Miner, test management logic and test execution logic are located within a microprocessor. However, this does not suggest that the same technique be applied to access a memory associated with an ASIC. Moreover, Miner does not teach or suggest a utility bus slave controller being used, particularly as part of the test management logic 570 as appears to have been analogized in the Final Office Action. Even if there were a bus controller within the management logic 570, it is clearly not suggested that it be a UBS controller as understood by one of ordinary skill in the art. Accordingly, reconsideration and withdrawal of the rejection of claim 30 is respectfully requested.

Any dependent claims not specifically mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims. In addition, although arguments have been made above to distinguish the claims from the relied upon art references, further arguments that may or may not refer to other aspects of a claim could be made, although they are not made at this time. A good faith attempt has, nevertheless, been made to address all rejections and to place the application in overall better condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on October 1, 2004.

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Margaux Rodriguez *October 1, 2004*